HMC708LP5 / 708LP5E

v04.0112

0.5 dB LSB 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, 1700 - 2200 MHz

Typical Applications

The HMC708LP5(E) is ideal for:

- Cellular Infrastructure
- WiBro, WiMAX and LTE/ 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors

Features

-2.5 to +29 dB Gain Control in 0.5 dB Steps

Power-up State Selection

High Output IP3: +37 dBm

Low Noise Figure: 1 dB

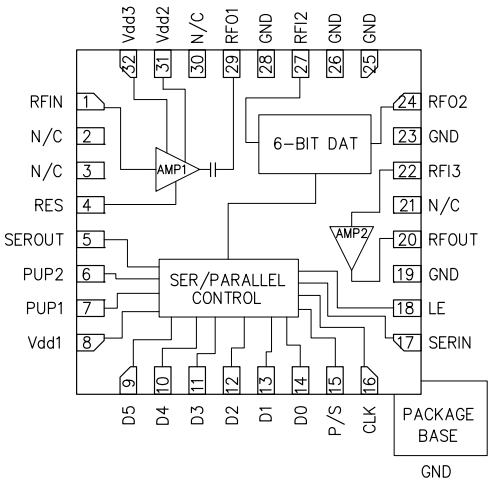
TTL/CMOS Compatible
Serial, Parallel, or Latched Parallel Control

±0.25 dB Typical Step Error

Single +3V and +5V Supply

32 Lead 5x5mm SMT Package: 25mm²

Functional Diagram



General Description

The HMC708LP5(E) is a digitally controlled variable gain amplifier which operates from 1700 MHz and 2200 GHz, and can be programmed to provide between 2.5 dB attenuation and +29 dB of gain, in 0.5 dB steps. The HMC708LP5(E) delivers noise figure of 1 dB in its maximum gain state, with output IP3 of up to +37 dBm. The dual mode gain control interface accepts either three wire serial input or 6 bit parallel word. The HMC708LP5(E) also features a user selectable power up state and a serial output for cascading other Hittite serially controlled components. For 900 MHz applications please refer to the HMC707LP5(E) data sheet.

Electrical Specifications, T_A = +25° C

Rbias = 270 Ohms for Vdd = +5V, Rbias = 10 kOhms for Vdd = +3V, Vdd = Vdd1 = Vdd2 = Vdd3

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Units
		Vdd = +3V			Vdd = +5V			
Frequency Range		1.7 - 2.2			1.7 - 2.2			GHz
Gain (Maximum Gain State)		23	27		25	30		dB
Gain Control Range			31.5			31.5		dB
Input Return Loss			16.5			20.5		dB
Output Return Loss			10.5			13.5		dB
Attenuation Accuracy: (Referenced to Maximum Gain State)		±(0.2 + 5%) of Attenuation Setting			±(0.2 + 5%) of Attenuation Setting			dB
Output Power for 1 dB Compression		13	16		18	21.5		dBm
Output Third Order Intercept Point (Two-Tone Input Power= -10 dBm Each Tone)			32.5			37.5		dBm
Noise Figure			1.1			1		dB
Switching Characteristics tRISE, tFALL (50% CTL to 90% RF)	tRISE		-			140		ns
	tFALL		-			270		ns
Current Amplifier 1		30	47	65	80	97	135	mA
Current Amplifier 2		130	155	190	130	155	190	mA

[1] Two-tone output power @ -10 dBm [2] Two-tone output power @ -5 dBm

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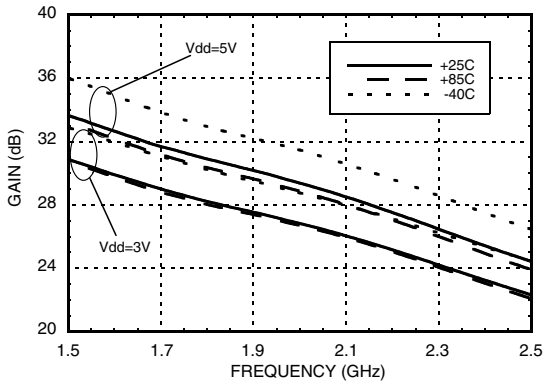
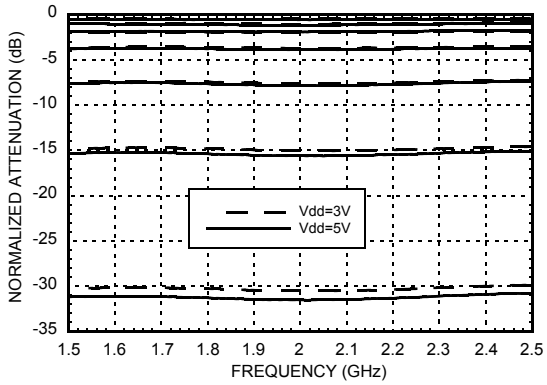
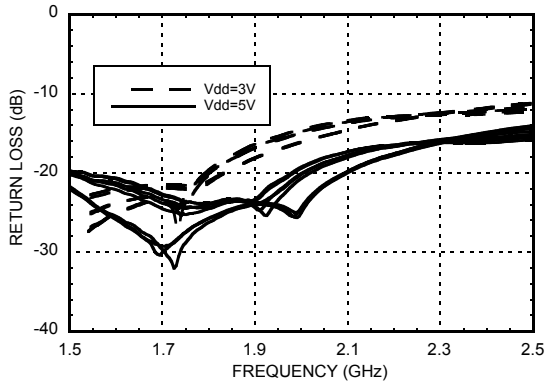
Maximum Gain vs. Frequency [1]



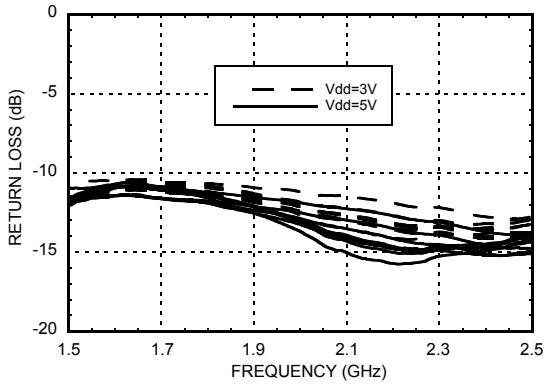
Normalized Attenuation
(Only Major States are Shown)



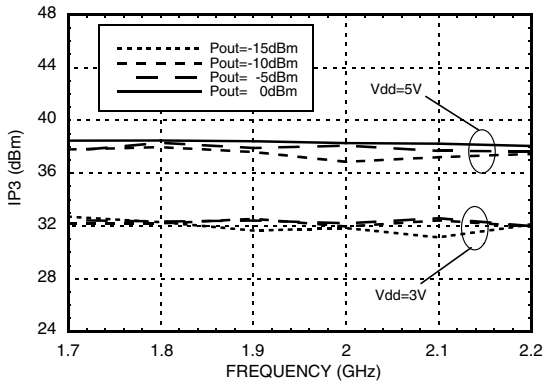
Input Return Loss
(Only Major States are Shown)



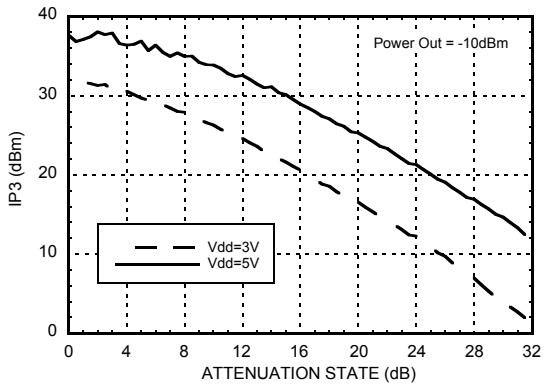
Output Return Loss
(Only Major States are Shown)



Output IP3 vs. Tone Power [1]



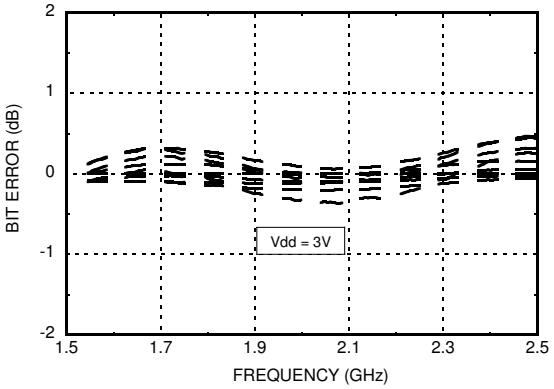
Output IP3 vs. Attenuation @ 1900 MHz



[1] Maximum gain state with digital attenuator set to minimum attenuation

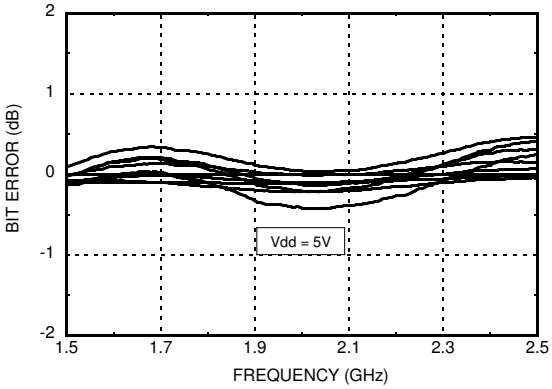
Bit Error vs. Frequency @ +3V

(Only Major States are Shown)

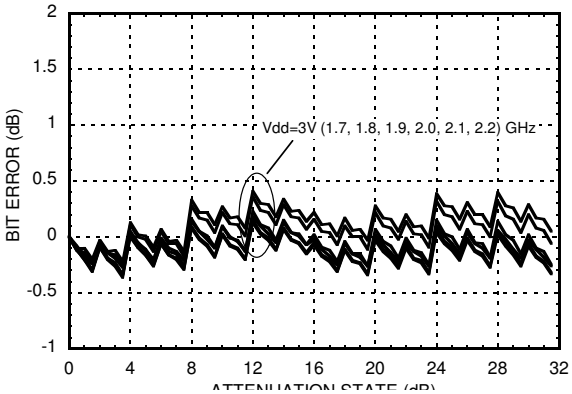


Bit Error vs. Frequency @ +5V

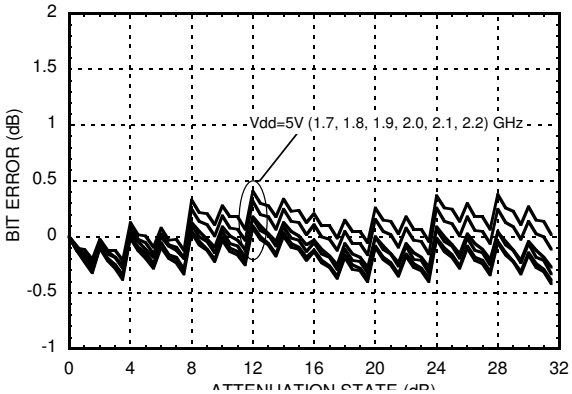
(Only Major States are Shown)



Bit Error vs. Attenuation State @ +3V

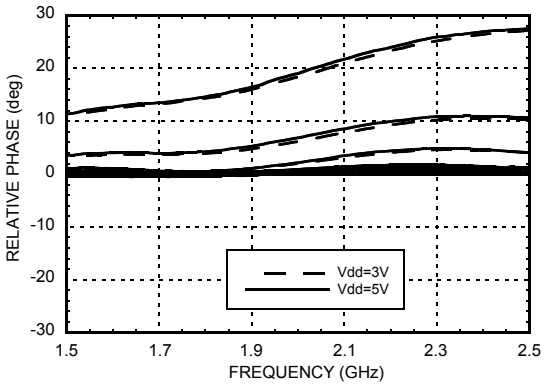


Bit Error vs. Attenuation State @ +5V



Normal Relative Phase vs. Frequency

(Only Major States are Shown)



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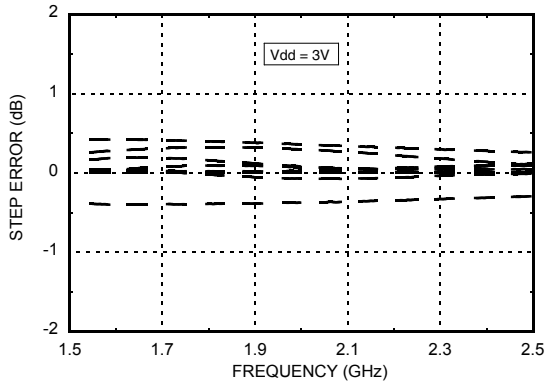
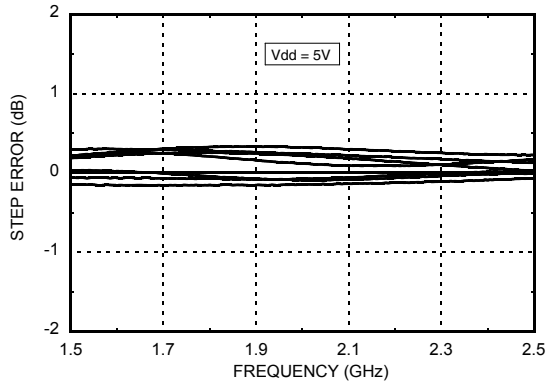
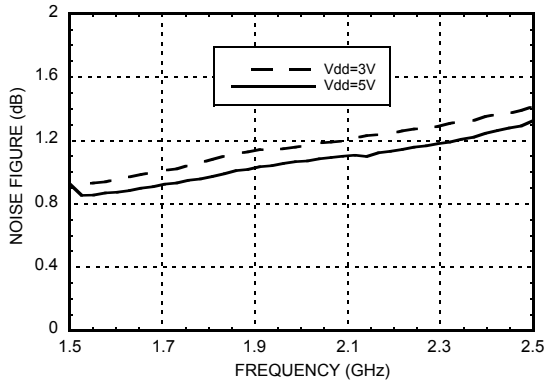
Step Error vs. Frequency @ +3V
(Only Major States are Shown)



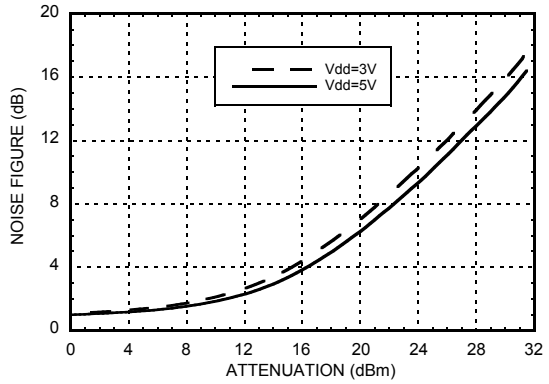
Step Error vs. Frequency @ +5V
(Only Major States are Shown)



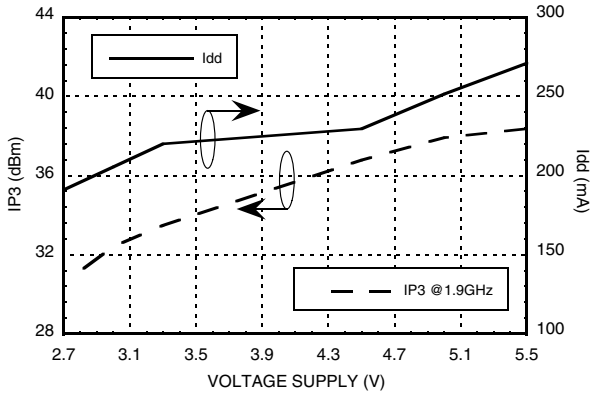
Noise Figure vs. Frequency



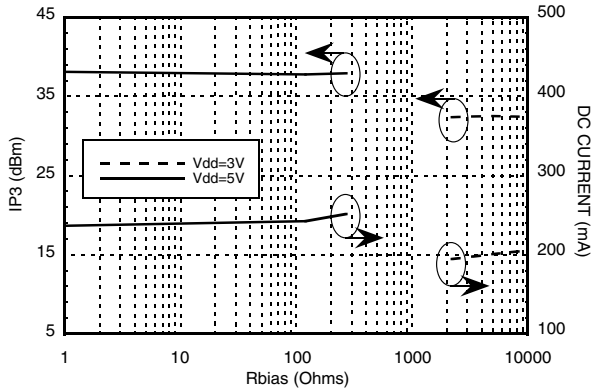
Noise Figure vs. Attenuation @ 1900 MHz



Output IP3 & Supply Current vs. Supply Voltage @ 1900 MHz

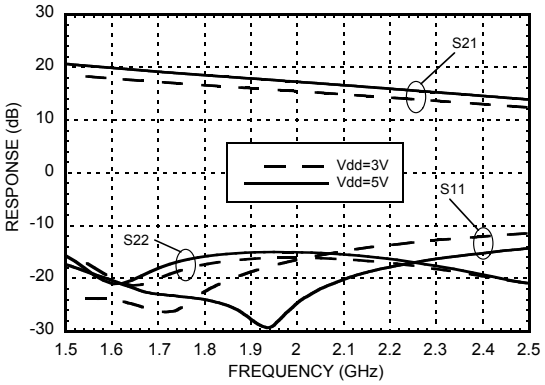


Output IP3 & Supply Current vs. Rbias @ 1900 MHz

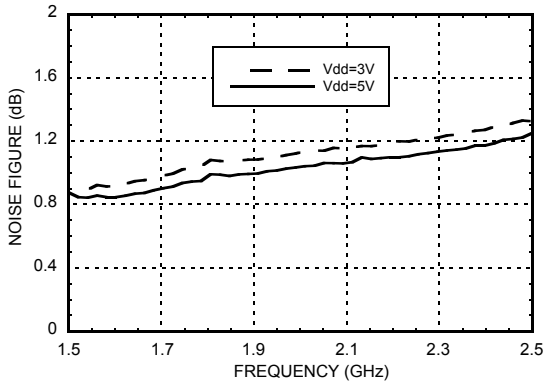


Option 1 [1] : Amp1 + 6-Bit DAT only

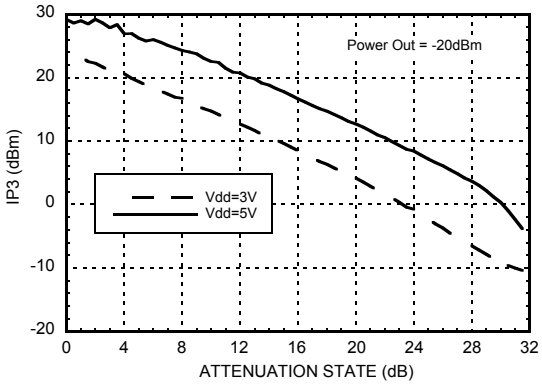
Gain & Return Loss [1] [2]



Noise Figure vs. Frequency [1] [2]



Output IP3 vs. Attenuation @ 1900 MHz [1]



[1] See Application Circuit [2] Maximum gain state with digital attenuator set to minimum attenuation

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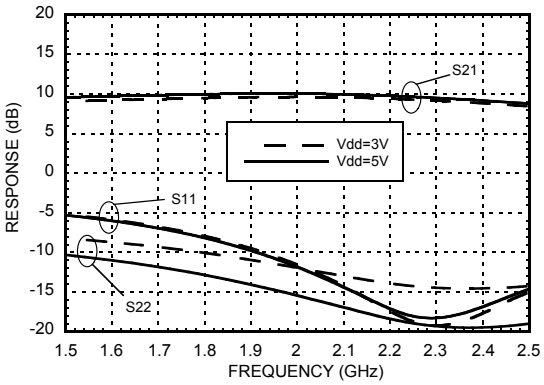
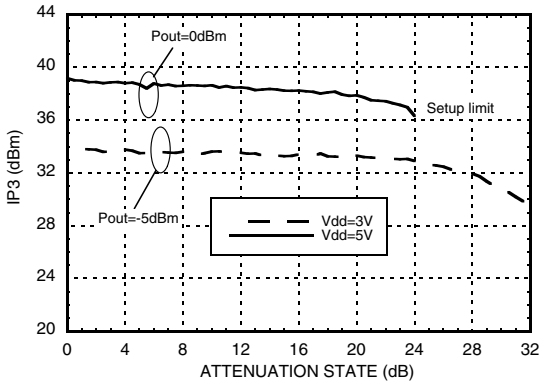
Option 2 [1] : 6-Bit DAT + Amp2 only

Gain & Return Loss [1] [2]



Output IP3 vs. Attenuation @ 1900 MHz [1]

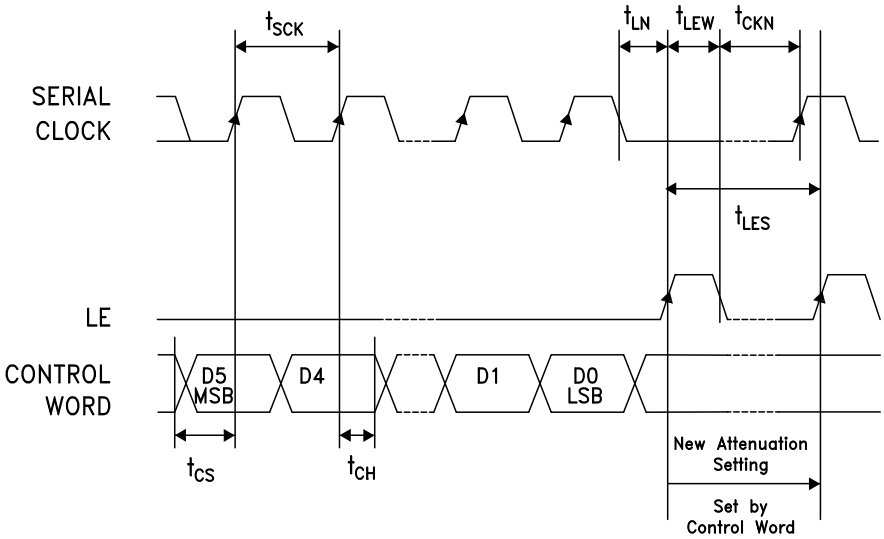


Serial Control Interface

The HMC708LP5(E) contains a 3-wire SPI compatible digital interface (SERIN, CLK, LE). It is activated when P/S is kept high. The 6-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. Standard logic families work well. If mechanical switches were used, sufficient debouncing should be provided. When LE is high, 6-bit data in the serial input register is transferred to the attenuator. When LE is high CLK is masked to prevent data transition during output loading.

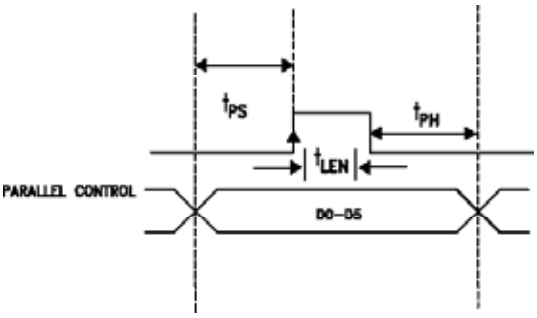
When P/S is low, 3-wire SPI interface inputs (SERIN, CLK, LE) are disabled and serial input register is loaded asynchronously with parallel digital inputs (D0-D5). When LE is high, 6-bit parallel data is transferred to the attenuator.

For all modes of operations, attenuation state will stay constant while LE is kept low.



[1] See Application Circuit [2] Maximum gain state with digital attenuator set to minimum attenuation

Timing Diagram *(Latched Parallel Mode)*



Parameter	Typ.
Min. serial period, t_{SCK}	100 ns
Control set-up time, t_{CS}	20 ns
Control hold-time, t_{CH}	20 ns
LE setup-time, t_{LN}	10 ns
Min. LE pulse width, t_{LEW}	10 ns
Min LE pulse spacing, t_{LES}	630 ns
Serial clock hold-time from LE, t_{CKN}	10 ns
Hold Time, $t_{PH.}$	0 ns
Latch Enable Minimum Width, t_{LEN}	10 ns
Setup Time, t_{PS}	2 ns

Parallel Mode *(Direct Parallel Mode & Latched Parallel Mode)*

Note: The parallel mode is enabled when P/S is set to low.

Direct Parallel Mode - The attenuation state is changed by the Control Voltage Inputs directly. The LE (Latch Enable) must be at a logic high to control the attenuator in this manner.

Latched Parallel Mode - The attenuation state is selected using the Control Voltage Inputs and set while the LE is in the Low state. The attenuator will not change state while LE is Low. Once all Control Voltage Inputs are at the desired states the LE is pulsed. See timing diagram above for reference.

Power-Up States

If LE is set to logic LOW at power-up, the logic state of PUP1 and PUP2 determines the power-up state of the part per PUP truth table. If the LE is set to logic HIGH at power-up, the logic state of D0-D5 determines the power-up state of the part per truth table. The DVGA latches in the desired power-up state approximately 200 ms after power-up.

Power-On Sequence

The ideal power-up sequence is: GND, Vdd, digital inputs, RF inputs. The relative order of the digital inputs are not important as long as they are powered after Vdd / GND

Control Voltage Table

State	Vdd = +3V	Vdd = +5V
Low	0 to 0.5V @ <1 µA	0 to 0.8V @ <1 µA
High	2 to 3V @ <1 µA	2 to 5V @ <1 µA

PUP Truth Table

LE	PUP1	PUP2	Gain Relative to Maximum Gain
0	0	0	-31.5
0	1	0	-24
0	0	1	-16
0	1	1	Insertion Loss
1	X	X	0 to -31.5 dB

Note: The logic state of D0 - D5 determines the power-up state per truth table shown below when LE is high at power-up.

Truth Table

Control Voltage Input						Gain Relative to Maximum Gain
D5	D4	D3	D2	D1	D0	
High	High	High	High	High	High	0 dB
High	High	High	High	High	Low	-0.5 dB
High	High	High	High	Low	High	-1 dB
High	High	High	Low	High	High	-2 dB
High	High	Low	High	High	High	-4 dB
High	Low	High	High	High	High	-8 dB
Low	High	High	High	High	High	-16 dB
Low	Low	Low	Low	Low	Low	-31.5 dB
Any combination of the above states will provide a reduction in gain approximately equal to the sum of the bits selected.						

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Typical Supply Current vs. Vdd (Rbias = 270Ω for Vdd= 5V, Rbias= 10kΩ for Vdd= 3V)

Vdd (V)	Total Idd (mA)
2.7	191
3.0	206
3.3	220
4.5	230
5.0	252
5.5	271

Note: Amplifier will operate over full voltage ranges shown above.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	5.5 V
RF Input Power (RFIN) (Vdd = +5 Vdc)	-5 dBm + Attenuation State (do not exceed +10 dBm)
Channel Temperature	150 °C
Digital Inputs ($\overline{\text{Reset}}$, Shift Clock, Latch Enable, Serial Input)	-0.5 to Vdd +0.5V
Continuous Pdiss (T= 85 °C) (derate 28 mW/°C above 85 °C)	1.8 W
Thermal Resistance (channel to ground paddle)	36.2 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Absolute Bias Resistor Range & Recommended Bias Resistor Values for Idd

Vdd	Rbias Ω			Total Idd (mA)
	Min.	Max.	Recommended	
3V	1K [1]	Open Circuit	2.2k	195
			4.7k	201
			10k	206
5V	0	Open Circuit	0	231
			120	243
			270	252

[1] Operation with Vdd= 3V and Rbias < 1K Ohm may result in the part becoming conditionally stable which is not recommended.

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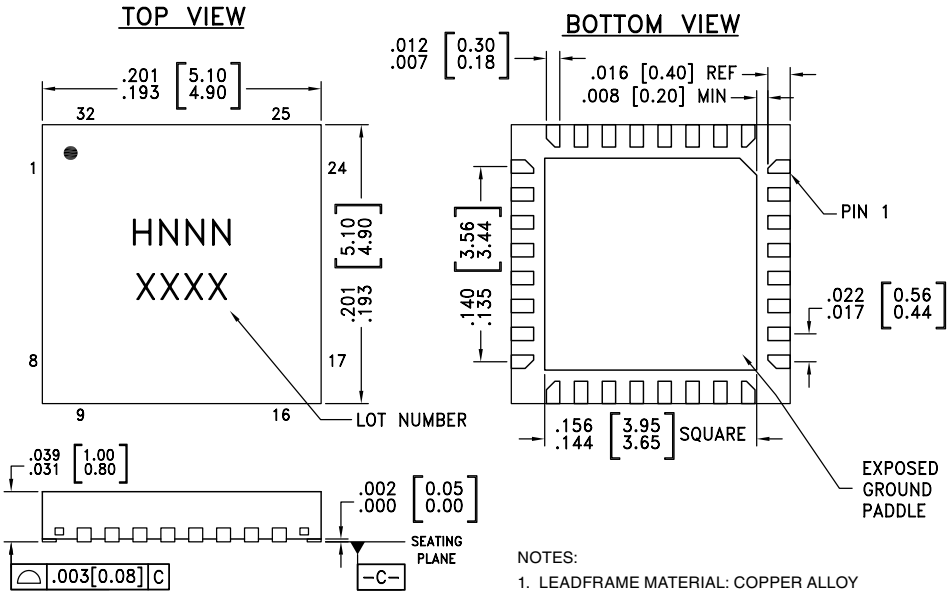
Outline Drawing



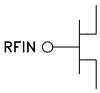
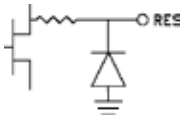
NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

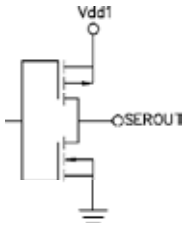
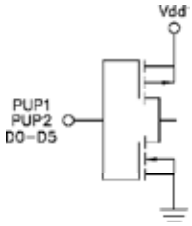
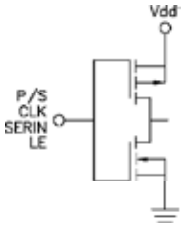
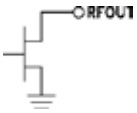
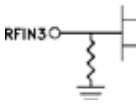
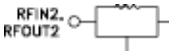
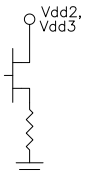
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC708LP5	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H708 XXXX
HMC708LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H708 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

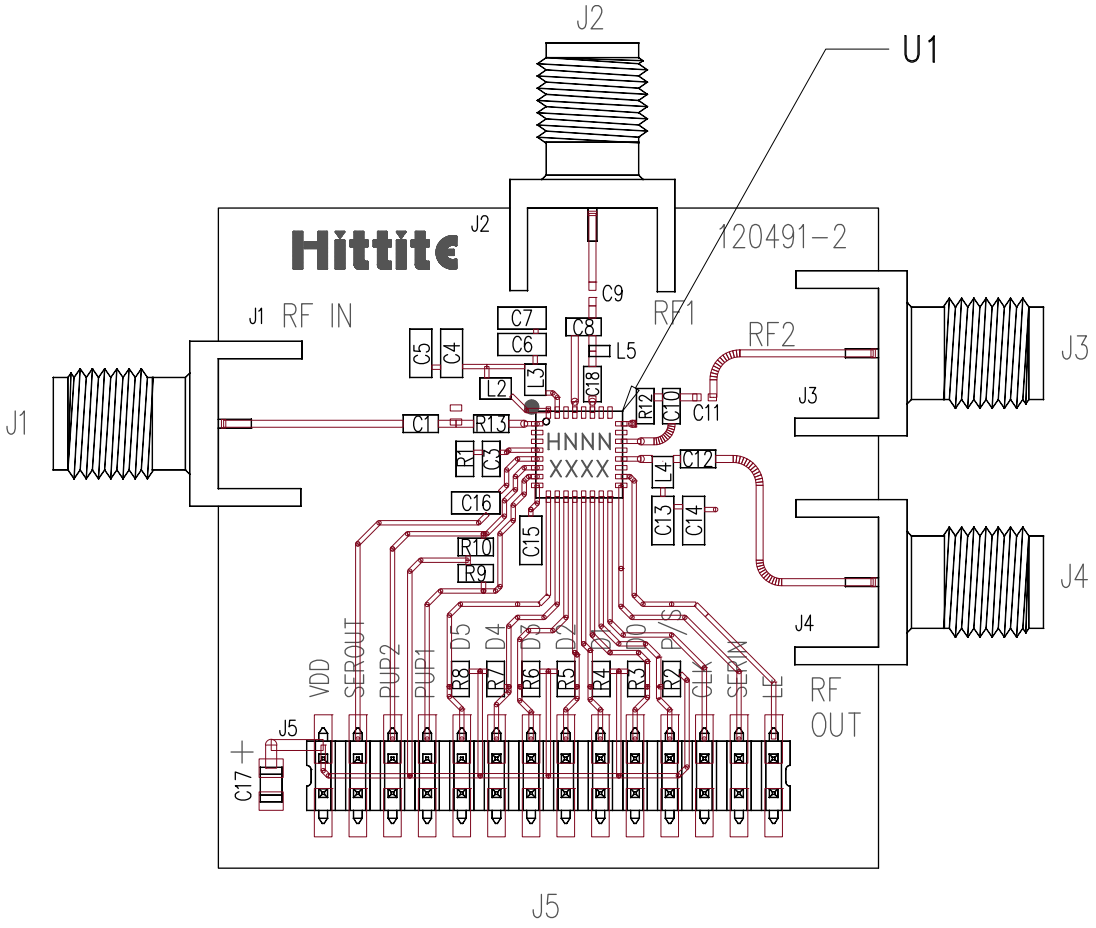
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	RFIN	RF input to the first amplifier (AMP1) This pin is DC coupled and matched to 50 Ohms.	
2, 3, 21, 30	N/C	No connection necessary. These pins may be connected to RF/DC ground without affecting performance.	
4	RES	This pin is used to set the DC current of the first amplifier by selection of external bias resistor. See application circuit.	

Pin Descriptions *(Continued)*

Pin Number	Function	Description	Interface Schematic
5	SEROUT	Serial input data delayed by 6 clock cycles.	
6, 7 9 - 14	PUP1, PUP2 D0 - D5	See truth table, control voltage table and timing diagram.	
8	Vdd1	Supply voltage	
15	P/S	See truth table, control voltage table and timing diagram.	
16	CLK		
17	SERIN		
18	LE		
19, 23, 25, 26, 28	GND	These pins and package bottom must be connected to RF/DC ground.	
20	RFOUT	RF Output and DC BIAS for the second amplifier (AMP2). See Application Circuit for off-chip components.	
22	RFIN3	RF input for the second amplifier (AMP2). This pin is DC coupled. An off-chip DC blocking capacitor is required.	
27	RFIN2	Input and output of the 6-bit digital attenuator (6-Bit DAT). These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
24	RFOUT2		
29	RFOUT1	RF output for the first amplifier (AMP1) This pin is matched to 50 Ohms.	
31, 32	Vdd2, Vdd3	Power Supply Voltage for the first amplifier. External bypass capacitors are required. See application circuit.	

Evaluation PCB



List of Materials for Evaluation PCB 120493 [1]

Item	Description
J1 - J4	PCB Mount SMA Connector
J5	2mm Vertical Molex 28pos Connector
C1, C8, C10, C12, C18	220 pF Capacitor, 0402 Pkg.
C3	10 nF Capacitor, 0402 Pkg.
C6, C13, C15	1000 pF Capacitor, 0603 Pkg.
C7, C14	10 nF Capacitor, 0603 Pkg.
C16	27 pF Capacitor, 0603 Pkg.
C17	4.7 uF Capacitor, 0805 Pkg.
L2	15 nH Inductor, 0402 Pkg.
L3	6.8 nH Inductor, 0603 Pkg.
L4	47 nH Inductor, 0603 Pkg.
L5	5.1 nH Inductor, 0402
R1 (Rbias)	270 Ohm Resistor, 0402 Pkg.
R2 - R10	39K Ohm Resistor, 0402 Pkg.

Item	Description
R12, R13	0 Ohm Resistor, 0402 Pkg.
U1	HMC708LP5(E) Variable Gain Amplifier
PCB [2]	120491 Evaluation PCB

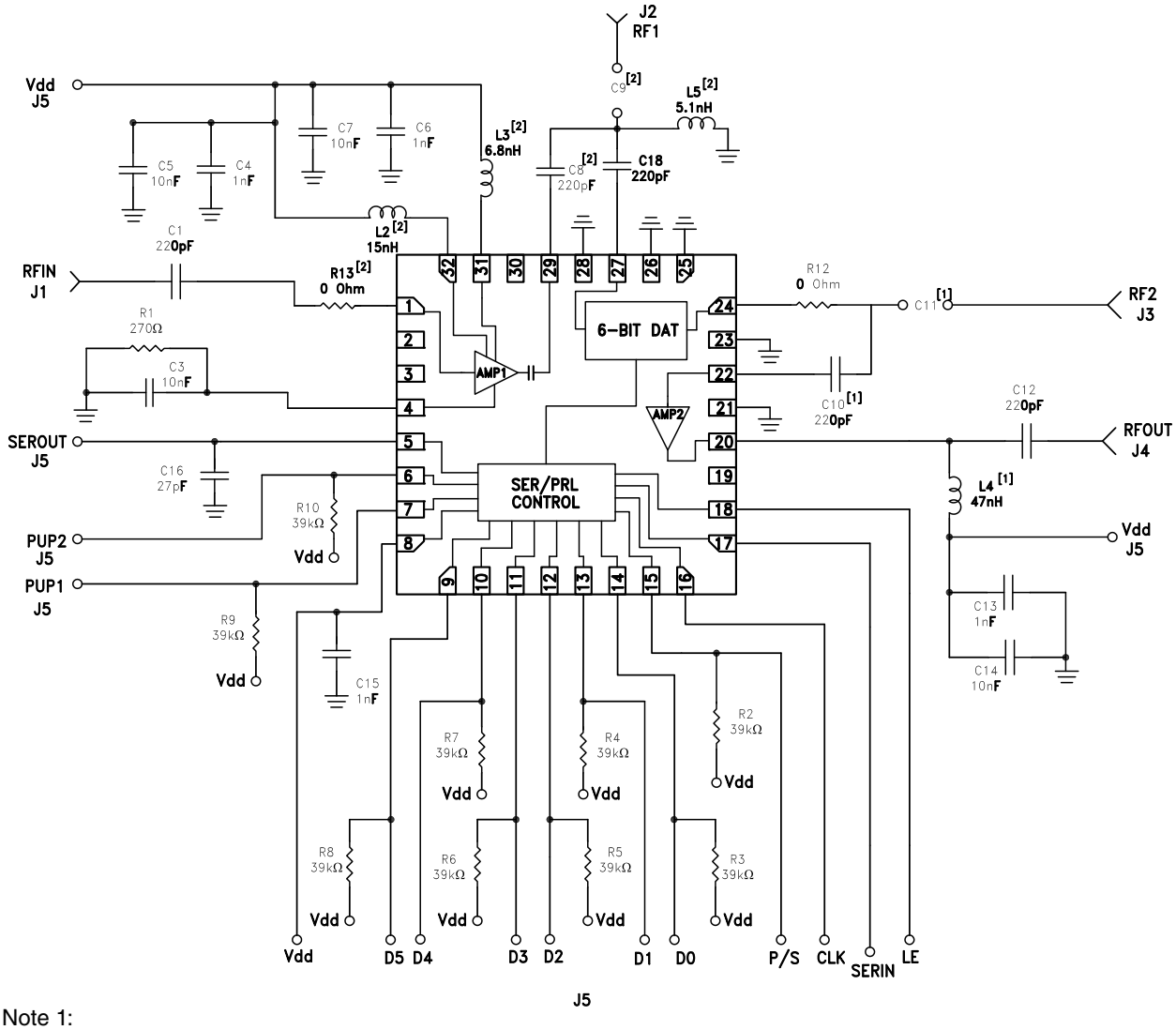
[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Roger 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

0.5 dB LSB 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, 1700 - 2200 MHz

Application Circuit



Note 1:
For option 1 (Amp1 + 6-bit DAT only) remove L4. Move 220pF capacitor (0402 Pkg.) from location C10 to C11.

Note 2:
For option 2 (6-Bit DAT + Amp2 only) remove R13, L2, L3 and L5. Move 220pF capacitor (0402 Pkg.) from location C8 to C9.